AMENDMENTS TO THE CLAIMS

The listing of claims below replaces all prior versions of claims in the application.

1. (Currently Amended): A method of manufacturing a semiconductor device comprising the steps of:

forming a resist pattern over a base layer;

applying a resist pattern smoothing material onto a surface of the resist pattern, thereafter heating and developing the resist pattern applied with the resist pattern smoothing material so as to form a smoothed resist pattern; and

etching the base layer using the smoothed resist pattern as a mask so as to form a pattern of the base layer,

wherein the resist pattern smoothing material comprises at least one of cationic surfactants~~, anionic surfactants,~~ and amphoteric surfactants,

wherein at least one of an application thickness of the resist pattern smoothing material and a heat temperature for the heating is adjusted in the range of 70nm to 90nm in thickness and in the range of 80°C to 95°C in temperature so as to smooth at least wall surfaces of the resist pattern,

wherein a maximum opening dimension Dmax (nm) and a minimum opening dimension Dmin (nm) of the smoothed resist pattern are within a range of ±5% with respect to an opening dimension D (nm) of the resist pattern opening according to an exposure process, and

wherein the opening dimension D (nm) of the resist pattern, and an average opening dimension Dav. (nm) of the smoothed resist pattern whose wall surfaces have been smoothed satisfy the relation expressed by:

$$Dav.\ (nm) \geq D\ (nm) \times (90/100).$$

2. (Cancelled)

3. (Original): A method of manufacturing a semiconductor device according to Claim 1, wherein a maximum opening dimension Dmax (nm) and a minimum opening dimension Dmin (nm) of the smoothed resist pattern are within a range of ± 3% with respect to a predetermined opening dimension D (nm) of the resist pattern.

4. (Cancelled)

5. (Original): A method of manufacturing a semiconductor device according to Claim 1, wherein a predetermined opening dimension D (nm) of the resist pattern, and an average opening dimension Dav. (nm) of the smoothed resist pattern whose wall surfaces have been smoothed satisfy the relation expressed by:

$$Dav.\ (nm) \geq D\ (nm) \times (95/100).$$

6. (Original): A method of manufacturing a semiconductor device according to Claim 1, wherein the resist pattern is formed of an ArF resist.

7. (Original): A method of manufacturing a semiconductor device according to Claim 1, wherein an opening dimension D (nm) of the smoothed resist pattern is within a range of 50 nm to 150 nm.

8. (Original): A method of manufacturing a semiconductor device according to Claim 1, wherein the heat temperature is within a range of 80 °C to 100 °C.

9. (Original): A method of manufacturing a semiconductor device according to Claim 1, wherein the application thickness of the resist pattern smoothing material is within a range of 70 nm to 100 nm.

10. (Previously Presented): A method of manufacturing a semiconductor device according to Claim 1 wherein the resist pattern smoothing material comprises a resin and a crosslinking agent.

11. (Original): A method of manufacturing a semiconductor device according to Claim 10, wherein the resist pattern smoothing material has one of water-solubility and alkali-solubility.

12-13. (Cancelled)

14. (Original): A method of manufacturing a semiconductor device according to Claim 10, wherein the resin is at least one of polyvinyl alcohol, polyvinyl acetal, and polyvinyl acetate.

15. (Original): A method of manufacturing a semiconductor device according to Claim 10, wherein the crosslinking agent is at least one of melamine derivative, urea derivative, and uril derivative.

16. (Original): A method of manufacturing a semiconductor device according to Claim 10, wherein the resist pattern smoothing material further comprises one of a water-soluble aromatic compound and a resin having an aromatic compound in a portion thereof.

17. (Original): A method of manufacturing a semiconductor device according to Claim 16, wherein the water-soluble aromatic compound is one of polyphenol compound, aromatic carboxylic acid compound, naphthalene polyhydric alcohol compound, benzophenone compound, flavonoid compound, derivatives thereof and glycosides thereof, and the resin containing an aromatic compound in a portion thereof is one of polyvinyl aryl acetal resin, polyvinyl aryl ether resin, and polyvinyl aryl ester resin.

18. (Original): A method of manufacturing a semiconductor device according to Claim 10, wherein the resist pattern smoothing material further comprises an organic solvent.

19. (Original): A method of manufacturing a semiconductor device according to Claim 18, wherein the organic solvent is at least one of alcohol solvent, chain ester solvent, cyclic ester solvent, ketone solvent, chain ether solvent, and cyclic ether solvent.

20. (Cancelled)

21. (Currently Amended): A method for manufacturing a semiconductor device comprising the steps of:

forming a resist pattern over a base layer;

applying a resist pattern smoothing material onto a surface of the resist pattern, thereafter heating and developing the resist pattern applied with the resist pattern smoothing material so as to form a ~~smothered~~ smoothed resist pattern; and

etching the base layer using the ~~smothered~~ smoothed resist pattern as a mask so as to form a pattern of the base layer,

wherein the resist pattern smoothing material comprises ~~polyoxyalklene alkylether~~ polyoxyethylene monoalkylether surfactant,

wherein the structure of the ~~polyoxyalklene alkylether~~ polyoxyethylene monoalkylether surfactant is a linear chain structure,

wherein at least one of an application thickness of the resist pattern smoothing material and a heat temperature for the heating is adjusted in the range of 70nm to 90nm in thickness and in the range of 80°C to 95°C in temperature so as to smooth at least wall surfaces of the resist pattern,

wherein a maximum opening dimension Dmax (nm) and a minimum opening dimension Dmin (nm) of the smoothed resist pattern are within a range of ±5% with respect to an opening dimension D (nm) of the resist pattern opening according to an exposure process, and

wherein the opening dimension D (nm) of the resist pattern, and an average opening dimension Dav. (nm) of the smoothed resist pattern whose wall surfaces have been smoothed satisfy the relation expressed by:

$$Dav.\ (nm) > D(nm) \times (90/100).$$

22. (Previously Presented): A method of manufacturing a semiconductor device according to claim 21, wherein a maximum opening dimension Dmax (nm) and a minimum opening dimension Dmin (nm) of the smoothed resist pattern are within a range of ± 3% with respect to a predetermined opening dimension D (nm) of the resist pattern.

23. (Previously Presented): A method of manufacturing a semiconductor device according to claim 21, wherein a predetermined opening dimension D (nm) of the resist pattern, and an average opening dimension Dav. (nm) of the smoothed resist pattern whose wall surfaces have been smoothed satisfy the relation expressed by:

$$Dav.\ (nm) \geq D\ (nm) \times (95/100).$$

24. (Previously Presented): A method of manufacturing a semiconductor device according to claim 21, wherein the resist pattern is formed of an ArF resist.

25. (Previously Presented): A method of manufacturing a semiconductor device according to claim 21, wherein an opening dimension D (nm) of the smoothed resist pattern is within a range of 50 nm to 150 nm.